FHI PLATFORM OMGEVINGSTECHNOLOGIE

Showcase

Next Generation Burn-In for advanced IC nodes

Evoluon Eindhoven, 21 November 2017

Kees Revenberg

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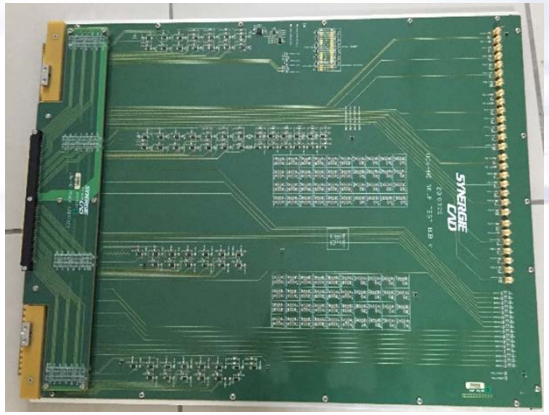
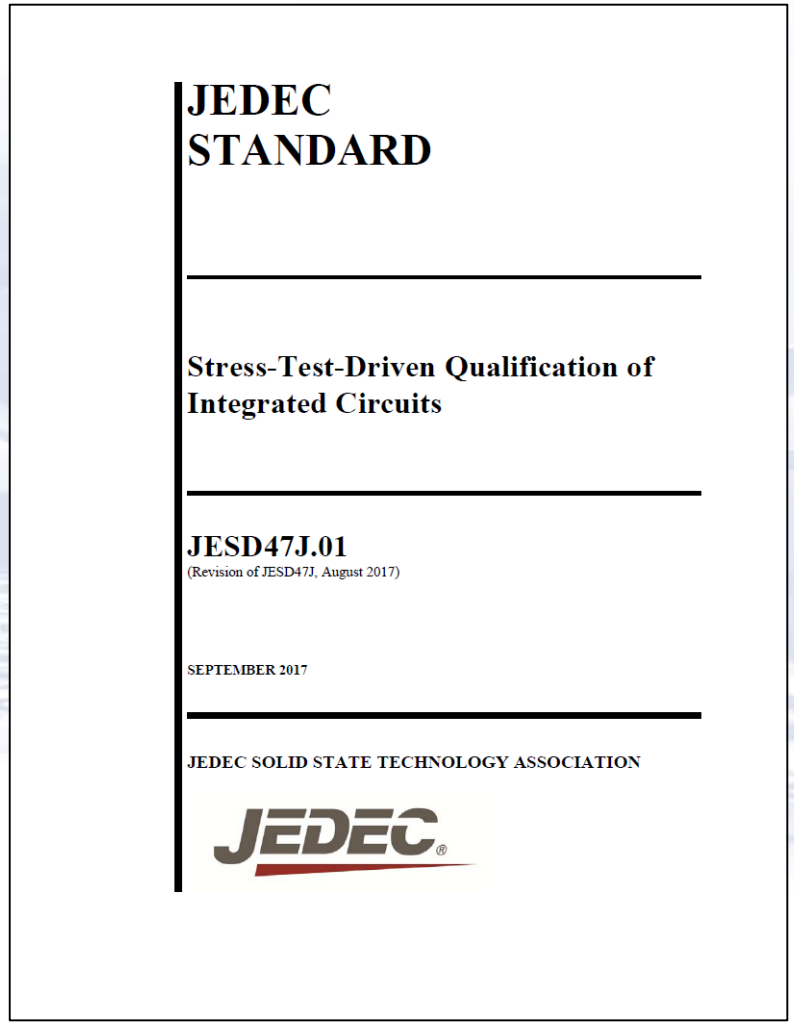


Company profile

- MASER Engineering is a Dutch based Independent Service Provider
- Advanced Failure Analysis capabilities
- Full Reliability Testing including all climatic, structural and ESD testing
- Well trained and experienced employees in Test and Diagnostics
- ISO 17025 accredited and ISO 9001 certified Lab
- Representations covering the EMEA area
- 24 years active since 1993
- One head office and twp EPA test and analysis laboratories in Enschede, NL

Introduction

- **Product Reliability Test procedure**
- **Standards like JEDEC 47 or AEC-Q100**
- **Thermally Induced Accelerated Life test**
  - High Temperature Operating Life [HTOL]
  - Low Temperature Operating Life [LTOL]
  - Power Cycling Test [PCT]
  - Power Temperature Cycling Test [PTC]
  - Early Life Failure Rate [ELFR]
- **Statistical data processing**
  - 3 wafer lots, 80 IC's per lot for HTOL
    - Acceptance level: 0 fails after 1000 hours @ +125°C
  - 3 wafer lots, 800 IC's per lot for ELFR
    - Acceptance level: $\chi^2/2$ distribution table
  - Based on equal conditions → Arrhenius model


JEDEC
STANDARD

Stress-Test-Driven Qualification of Integrated Circuits

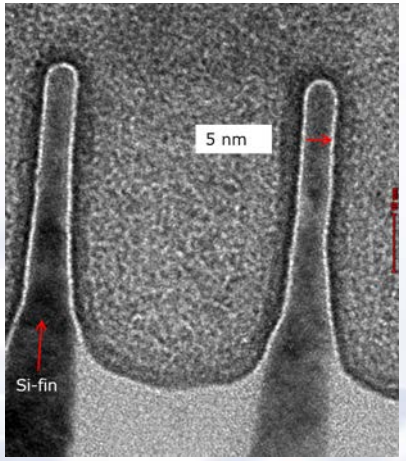
JESD47J.01
(Revision of JESD47J, August 2017)

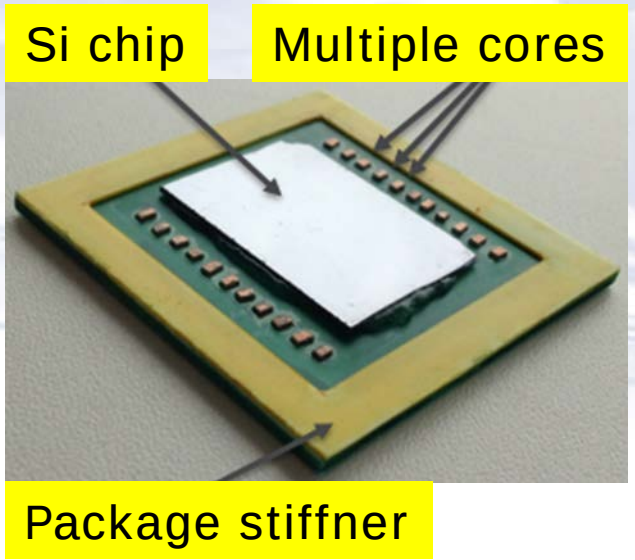
SEPTEMBER 2017

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

Advanced IC nodes

- Smaller geometries → 7 / 10nm node
- New transistor materials, construction and behavior
- Small process changes → big difference in behavior
- Higher speed → more power dissipation
- Increase of Tj deviation at die to die <100nm node
- Advanced processors
  - High pin count → >2000
  - High number of (FinFet) transistors → >1.000.000.000
  - High current consumption → >50A per core voltage
  - Low core voltage → <1,0V
- Special tools to balance IC by IC parameters
  - Individual Tj control and complex vector stimuli





High Temperature Operating Life Test

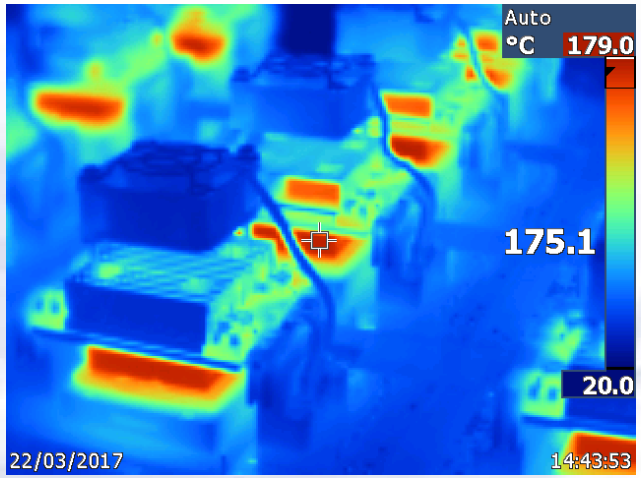
- **Temperature chamber**
  - Large chamber for square burn-in boards
  - Wide temperature range: -20°C to +175°C
  - Multiple thermal zones for parallel project execution
  - High ventilation speed in order to absorb sufficient heat
- **Flexible and Configurable**
  - 1:1 programmable driver to burn-in board wall connection
  - Wide range of serial data protocol and power supply controllers
  - Integrated Temperature Controlle Socket (TCS) and voltage/current/signal monitoring
- **Signal and Power distribution**
  - SPIL converted ATE vectors
  - High current at Low voltage power distribution
  - High data rate and digital signal generators

Synergie CAD system

- **Next Generation HTOL system**
  - UDx-700 system of Synergie CAD as next generation HTOL system
  - Debug station operational for trail and Burn-In Board evaluation
  - i-Socket module based HTOL board for SoC 28nm device
  - 1000 hours @ +175°C with 0/12 result, no failures

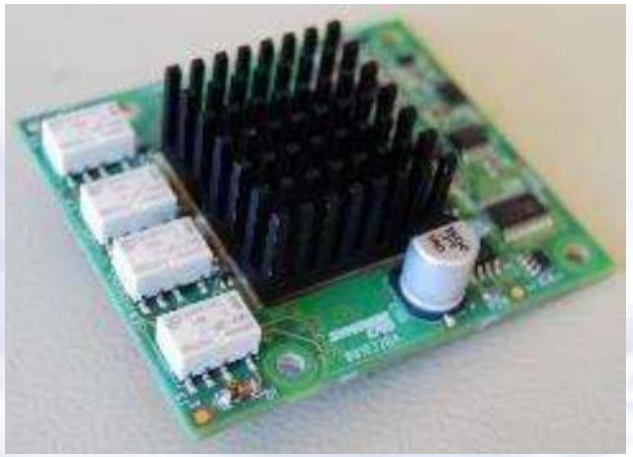
Synergie CAD system

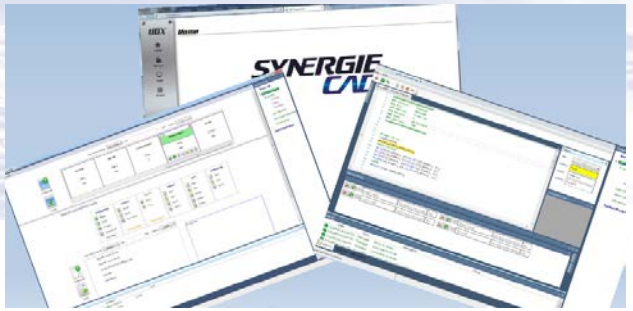
- **UDx-700 specifications – 1**
  - Multiple chamber styles
    - L2.12 2 thermal zones × 12 slots
    - L2.5 2 thermal zones × 5 slots
    - L4.5 4 thermal zones × 5 slots
    - 1:1 driver to BIB ratio
    - 50mm slot pitch
    - Ambient Temperature -40..180°C
  - Board style
    - 450 × 580 × 1.6mm (4× larger than half-Triotech)
    - 3×180 edge fingers + stacked 160-pin power nail connector
  - 65 Power Supply Unit slots per driver
    - Normal: **5A** @ **15V** (1 slot per module)
    - Special: **10A** @ 10V (2 slots per module)
    - Special: **20A** @ 10V (4 slots per module)
    - Special: 0.5A @ **100V** (1 slot per module)
    - Per driver max 248A / 800W



Synergie CAD system

- **UDx-700 specifications – 2**
  - 320 channels
    - up to 160 for monitoring, also analog voltage
    - clock 20 MHz (50 to 500 MHz upon request)
    - > 100Mb deep pattern through SSD on each driver
  - 24 on-board function generators
    - 12× sine/square 100 Hz - 53 MHz
    - 4× sine/square/diff 100 Hz - 20 MHz
    - 4× AWG
    - 4× 32.768 kHz square
  - Protocol communication with on-board µC
    - SPI, I^2C, JTAG, UART, etc.
    - Custom protocols can be defined
  - Intuitive software
    - Smart recipe management and compilation
    - Pattern development and import (STIL, WGL, VCD…)
    - Webbased software for monitoring





Summary

- Next generation burn-in system selected
- Addresses both necessary flexibility and configurability
- Prepared for current and future semiconductor nodes
- Ready for build-in test and scan path on chip facilities
- Debug station for board and program verification
- Full system delivered in Q1-2018, projects in Q2-2018
- Board design started already

Thank you for your attention!

Questions can be addressed at sales@maser.nl